IN THE CLAIMS:

Rewrite the pending claims and add new claims as follows:

1-37. (Canceled).

38. (Currently Amended) A memory system, comprising:

a communication channel coupled to a master memory device and coupled to a slave memory device;

the master memory device configured to generate control information and associated data information including a plurality of write commands with associated write information for each write command to the slave memory device followed by any operation code other than a read or write command to the slave memory device and then followed by a read command to the slave memory device; and

the slave memory device configured to receive the control information and associated data information in a same order as generated by the master memory device and to process the read command delayed according to the operation code other than a read or write command to the slave memory device prior to completing the processing of at least one of the plurality of write commands without causing a column resource conflict at a memory core of the slave memory device.

39. (Previously presented) A memory system, comprising:

a communication channel coupled to a master memory device and coupled to a slave memory device;

the master memory device configured to generate control information and associated data information including a plurality of write commands with associated write information for each write command to the slave memory device followed by any operation code other than a read or write command to the slave memory device and then followed by a read command to the slave memory device; and

the slave memory device configured to process the read command prior to completing the processing of at least one of the plurality of write commands without causing a column resource conflict at a memory core of the slave memory device;

wherein the slave memory device includes:

a write data buffer to store the associated write information of at least one of the plurality of write commands, the write buffer configured to receive the associated write

information in a first step and to retire the associated write information from the write data buffer to the memory core of the slave memory device in a second step.

40. (Original) The memory system of claim 39 wherein the master memory device is further configured to generate a first distinct control signal to indicate the transport of the associated write information to the write data buffer in the first step and a second distinct control signal to indicate the retirement of the associated write information to the memory core of the slave memory device in the second step.

41. (Original) The memory system of claim 39 wherein the slave memory device is configured to retire the associated write information from the write data buffer to the memory core of the slave memory device when a read command is not being processed at the memory core.

42. (Original) The memory system of claim 39 wherein the write data buffer is configured to retire the associated write information in response to any control information other than one associated with processing a read command to the slave memory device.

43. (Original) The memory system of claim 39 wherein the write data buffer is configured to retire the write data information in the absence of any control information.

44. (Original) The memory system of claim 39 wherein the write data buffer is positioned in the slave memory device.

45. (Original) The memory system of claim 39 wherein the write data buffer is positioned in the master memory device.

46. (Currently amended) A method of operating a memory system with a master memory device coupled to a slave memory device, the method comprising:

generating with the master memory device control information and associated data information including a plurality of write commands with associated write information for each write command to the slave memory device followed by any operation code other than a read or write command to the slave memory device and then followed by a read command to the slave memory device;

receiving the control information and associated data information in the slave memory device in a same order as generated by the master memory device;

processing the read command at the slave memory device; and

completing the processing of at least one of the plurality of write commands at the slave memory device after processing the read command delayed according to the operation code other than a read or write command to the slave memory device so as to avoid a column resource conflict at a memory core of the slave memory device.

47. (Previously presented) A method of operating a memory system with a master memory device coupled to a slave memory device, the method comprising:

generating with the master memory device control information and associated data information including a plurality of write commands with associated write information for each write command to the slave memory device followed by any operation code other than a read or write command to the slave memory device and then followed by a read command to the slave memory device;

transporting the associated write information of at least one of the plurality of write commands into a write data buffer;

processing the read command at the slave memory device; and

completing the processing of at least one of the plurality of write commands at the slave memory device after processing the read command so as to avoid a column resource conflict at a memory core of the slave memory device.

48. (Original) The method of claim 47 wherein the transporting step is indicated by a distinct transport control signal.

49. (Original) The method of claim 47 wherein the completing step further comprises:

retiring the associated write information from the write data buffer to the memory core of the slave memory device wherein the associated write information is retired into the memory core when a read command is not being processed at the memory core.

50. (Original) The method of claim 49 wherein the retiring step is indicated by a distinct retire control signal.

51. (Original) The method of claim 49 wherein the retiring step is performed in response to any control information other than control information associated with processing of a read command to the slave memory device.

52. (Original) The method of claim 49 wherein the retiring step is performed in the absence of any control information.

53. (Currently amended) The method of claim ~~46~~ 47 wherein the transporting step is performed in the slave memory device.

54. (Currently amended) The method of claim ~~46~~ 47 wherein the transporting step is performed in the master memory device.